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TITLE: METHOD AND APPARATUS TO PERFORM ON-DIE
                    WAVEFORM CAPTURE

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FIELD

Embodiments of the present invention may relate to testing of circuits.

5   More particularly, embodiments of the present invention may relate to the capture

of waveforms on a die or chip.

BACKGROUND

Within electronic systems, integrated circuits may communicate with each

10   other using electrical signals that travel through electrical conductors.   During

testing of electronic systems, the electrical conductors may be probed with test

equipment to verify that electrical signals exhibit desired characteristics.   For

example, signal characteristics such as voltage amplitude and time delay may be

measured using test equipment.

15   Test equipment probes may have an effect on electrical signals when

conductors are probed. For example, capacitive effects of a probe may distort a

signal when the probe is placed upon an electrical conductor through which the

signal travels. This can result in measurement errors in part because the signal

is being distorted by the test equipment.

20   As the size of electronic systems decrease, and as the speeds with which

they operate increases, the signal distorting effects of test equipment can

become more pronounced.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and a better understanding of the present invention will become apparent from the following detailed description of arrangements and example embodiments and the claims when read in connection with the

5   accompanying drawings, all forming a part of the disclosure of this invention. While the foregoing and following written and illustrated disclosure focuses on disclosing arrangements and example embodiments of the invention, it should be clearly understood that the same is by way of illustration and example only and the invention is not limited thereto.

10   The following represents brief descriptions of the drawings in which like reference numerals represent like elements and wherein:

FIG. 1 illustrates two integrated circuits coupled together according to an example arrangement;

FIG. 2 shows a captured waveform according to an example arrangement;

15   FIG. 3 is a flowchart showing a waveform capturing methodology according to an example arrangement;

FIG. 4 shows an I/O receiver having a filtering and waveform capturing methodology for one channel according to an example embodiment of the present invention;

20   FIG. 5 is a circuit diagram of a V-I converter and current multiplier according to an example arrangement;

FIG. 6 is a circuit diagram of a V-I converter, current multiplier and latch device according to an example embodiment of the present invention;

FIG. 7 is a system level block diagram according to an example embodiment of the present invention; and

5   FIG. 8 is a system level block diagram according to an example embodiment of the present invention.

DETAILED DESCRIPTION

In the following detailed description, like reference numerals and

10   characters may be used to designate identical, corresponding or similar components in differing figure drawings. Further, in the detailed description to follow, example sizes/models/values/ranges may be given although the present invention is not limited to the same. Well-known power/ground connections to integrated circuits (ICs) and other components may not be shown within the

15   FIGs. for simplicity of illustration and discussion. Further, arrangements and embodiments may be shown in block diagram form in order to avoid obscuring the invention, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements may be dependent upon the platform within which the present invention is to be implemented. That is, the

20   specifics are well within the purview of one skilled in the art. Where specific details are set forth in order to describe example embodiments of the invention, it

should be apparent to one skilled in the art that the invention can be practiced without these specific details.

Embodiments of the present invention may relate to waveform capture on a receiver (or receiving device) that performs signal modification(s) such as

5   filtering. For example, embodiments of the present invention may be applicable to testing of channel performance. Embodiments of the present invention are therefore applicable to reconstructing a channel response in order to perform waveform capturing.

Waveform capturing may be used to perform system level characterization

10   and produce diagrams (i.e., eye diagrams) useful during testing (or measurement) of circuits (such as integrated circuits). Waveform capturing may also be used to perform interconnect characterization by averaging out any source of circuit noise and jitter. Waveform capturing may be used with any device that uses high-speed input/output (I/O).

15   FIG. 1 illustrates two integrated circuits coupled together according to an example arrangement. Other arrangements are also possible. More specifically, FIG. 1 shows an integrated circuit 10 and an integrated circuit 50 coupled together by a conductor 70. In operation, the integrated circuit 10 may source a waveform on an output node 12. The waveform travels through the conductor 70

20   and is received by the integrated circuit 50 at an input node 52. The integrated circuit 10 may include a multiplexer 16 to select a data source from either outbound data on a node 18, or a repetitive waveform on a node 20. The

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outbound data on the node 18 may be sourced by other circuits (not shown) in the integrated circuit 10, and may represent data to be transferred between integrated circuits during normal operation. For example, the multiplexer 16 may select outbound data from a register file, an arithmetic logic unit (ALU), a memory

5   device, or any other functional block within the integrated circuit 10. The repetitive waveform may be selected by the multiplexer 16 to provide a repetitive waveform on the conductor 70 to be captured, in whole or in part, by the integrated circuit 50.

The integrated circuit 50 includes a sampler 54, a receiver 56, internal

10   circuits 58, a storage mechanism 60, and a control mechanism 62. The sampler 54 may sample the waveform received on the input node 52 in response to the variable clock signal sourced by the control mechanism 62. The sampler 54 may provide the waveform sample to the receiver 56 on a node 55. The receiver 56 may compare an amplitude of the waveform sample on the node 55 to a variable

15   threshold on the node 64, and provide a digital output to either or both of the internal circuits 58 or the storage mechanism 60. The internal circuits 58 may represent any circuitry within the integrated circuit 50 that receives data from the receiver 56 during normal operation. For example, the internal circuits 58 may include registers, memory, graphics devices, or any other functional blocks within

20   the integrated circuit 50. The storage mechanism 60 may be used to store information related to "waveform-capture" mode.

The receiver 56 may be one of many different types. For example, the receiver 56 may include an amplifier with a single-ended input to receive the waveform sample on the node 55, and a reference voltage input to receive a reference voltage on the node 64. The receiver 56 may also include a variable

5   offset comparator with a differential input to receive a differential input signal on the node 55. The node 55 may also include two conductors to carry a differential signal. The variable threshold on the node 64 may be a reference voltage to be compared against the waveform sample on the node 55, or may be a control signal that specifies a threshold or reference to be used within the receiver 56.

10   For example, the variable threshold on the node 64 may include a digital word that specifies an offset to be utilized within a variable offset comparator that has a differential input.

The control mechanism 62 may provide a variable clock signal to the sampler 54 on a node 66 and a variable threshold to the receiver 56 on the node

15   64. The control mechanism 62 may be any type of circuit capable of providing the variable clock and variable threshold, and capable of communicating with the storage mechanism 60. For example, the control mechanism 62 may include a microprocessor, a state machine, or the like. The control mechanism 62 may also include a voltage reference circuit. The control mechanism 120 may also

20   include a memory-mapped interface to allow an external device to access the capabilities of the control mechanism 62.

Each of the integrated circuits 10 and 50 may operate in one of two modes: an "operational" mode, and a "waveform-capture" mode. In the operational mode, the integrated circuit 10 may source data onto the conductor 70 from the outbound data node 12. This data, as described above, may be from

5   any source within the integrated circuit 10. Also in the operational mode, the sampler 54 may sample the signal waveform on the conductor 70 at the appropriate time and present the waveform sample to the receiver 56. The receiver 56 may convert the waveform sample to digital data, and the digital data may be sent on to the internal circuits 58.

10   In the operational mode, the control mechanism 62 may source a clock signal that allows the sampler 54 to sample the incoming waveform at a time point that provides an adequate timing margin. For example, for a four gigabit per second (4Gb/s) data link, the sampler 54 may sample every 250 picoseconds (ps) near the center of each bit cell. Also in the operational mode, the control

15   mechanism 62 may source a threshold value to the receiver 56 that provides adequate timing margin. The control mechanism 62 may use information gathered in the waveform-capture mode (described below) to determine the appropriate threshold value for operational mode.

The operational mode may be used when the integrated circuits 10 and 50

20   are performing normal functions as part of an electronic system. For example, the integrated circuit 10 may be a microprocessor, and the integrated circuit 50 may be a peripheral device coupled to the microprocessor, where both are part

of a computer system. The operational mode may be used when the computer is operating normally, and the integrated circuit 10 is transmitting data to the integrated circuit 50 as part of normal computer operation.

In the waveform-capture mode, the integrated circuit 10 may provide a
5   repetitive waveform on the conductor 70, and the integrated circuit 50 may repeatedly sample the waveform at various times and compare the sampled waveform to various thresholds to "capture" the waveform. The repetitive data provided by the integrated circuit 10 can be any repeating data stream, such that the integrated circuit 50 can sample the "same" time point of the waveform
10   relative to a fixed point in the repeating pattern. For example, the repetitive data may be produced by a linear feedback shift register (LFSR), a state machine, a shift register preloaded with data of interest, or the like.

In at least one example arrangement, a first-in-first-out (FIFO) register may be configured to produce a repetitive pattern every 80 bits. In another
15   example arrangement, shorter or longer patterns may be used. During the waveform-capture mode, the waveform that is captured may correspond to a portion of the repeating waveform, or the entire repeating waveform.

The control mechanism 62 may provide the variable clock to the sampler 54 on the node 66 to allow the sampler 54 to vary the time at which a waveform
20   sample is taken. In some arrangements, the variable clock may be varied over at least one bit cell period. For example, for a four gigabit per second (4Gb/s) data link, the variable clock may be varied over at least 250 picoseconds (ps). In

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some arrangements, the variable clock signal can be varied with approximately 9ps resolution.

The control mechanism 62 may also provide the variable threshold to the receiver 56 on the node 64. The receiver 56 may produce a digital signal that is

5 the result of an amplitude comparison between the sampled waveform on the node 55 and the variable threshold on the node 64. Accordingly, the variable threshold causes the receiver 56 to change the received signal level below which a digital "0" is output, and above which a digital "1" is output.

By varying the variable clock and the variable threshold in a coordinated

10 fashion, the control mechanism 62 may cause the "capture" of all or part of the repetitive waveform received on the input node 52. For each time point in a repetitive waveform, the control mechanism 62 may vary the threshold to take multiple measurements of the same point in the repeating waveform.

FIG. 2 shows a captured waveform 200 according to one arrangement.

15 Other arrangements are also possible. In the graph of FIG. 2, the vertical axis represents amplitude and the horizontal axis represents time. The waveform 200 corresponds to a portion of a repeating waveform. For example, the waveform 200 may correspond to a 135 ps section of a repeating waveform on the conductor 70 (FIG. 1) sampled at 9 ps intervals. The waveform 200 may be

20 captured and stored within the storage mechanism 60.

FIG. 3 is a flowchart showing a waveform capturing methodology according to an example arrangement. Other operations, orders of operations

and arrangements are also possible. FIG. 3 will be described with respect to elements of FIG. 1 and the graph and waveform shown in FIG. 2.

In block 310, a transmitter may send a periodic and repeatable waveform to a receiver. This may correspond to the integrated circuit 10 sending a

5   repetitive waveform on the conductor 70 to the integrated circuit 70 (FIG. 1). In block 320, the receiver synchronizes to the repeating waveform such that time points within the waveform can be repeatedly sampled. This may correspond to the control mechanism 62 receiving the clock signal on a node 68 (FIG. 1). This may also correspond to a clock recovery loop circuit (not shown) to generate a

10   clock signal.

In block 330, the variable clock may be set to sample the repetitive waveform at the first time point of interest. This time point may correspond to a time 214 (FIG. 2). In block 340, the variable threshold may be set to a first value corresponding to an amplitude 212 shown in FIG. 2. In block 350, the repeating

15   waveform may be sampled a number of times at the current time point, and the waveform sample may be compared against the current threshold to produce a digital "0" or a digital "1". In block 352, the number of digital "1"s or the number of digital "0"s output by the receiver 56 may be stored in the storage mechanism 60.

In block 354, the threshold may be incremented, and the actions in blocks

20   350 and 352 may be repeated for the new threshold. Block 356 tests the threshold level, and blocks 350, 352, and 354 may be repeated until the

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threshold has been incremented to the last point of interest, shown in FIG. 2 as an amplitude 216.

When the threshold is initialized at a low amplitude, it is more likely that the receiver 56 will output a digital "1" than a digital "0" because the amplitude of

5   the waveform is clearly above the threshold. Likewise, when the threshold is at a high amplitude, it is more likely that the receiver 56 will output a digital "0" than a digital "1" because the amplitude of the waveform is clearly below the threshold. As the threshold is increased towards the amplitude of the waveform from below, the likelihood increases that the receiver 56 will output a digital "0" rather than a

10 digital "1". This information is stored as a "distribution" in the storage mechanism 60 after the operations in blocks 340, 350, 352, and 354 are performed for a given time point.

In block 360, the distribution stored in the storage mechanism 60 may be differentiated to create a probability density function (pdf) of the uncertainty in the

15 waveform. This uncertainty can be caused by many different factors, including but not limited to, jitter, voltage noise, or noise present in the receiver 56.

In block 365, the mean of the pdf for each time point is calculated to determine the most likely amplitude position of the waveform at each time point. The mean of the pdf for the first time point 214 is shown at point 206.

20 In block 370, the variable clock may be incremented, and the actions in blocks 350 and 352 are repeated for the new threshold. Block 375 tests the time point, and blocks 340, 350, 352, 354, 356, 360, 365, and 370 are repeated until

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the clock has been incremented to the last time point of interest, shown in FIG. 2, as a time point 224. This corresponds to sampling the waveform multiple times for each threshold at each time point shown in FIG. 2, storing the likelihood information for each threshold, creating the pdf for the time point, and calculating

5   the mean of the pdf.

The captured waveform may then be reconstructed in block 380 by interpolating between the means at each time point. In FIG. 2, the captured waveform is shown as curve 210.

Waveform capturing will now be described with respect to filtering

10   performed on the receiver side of a transmission line. These techniques may occur within an integrated circuit such as the integrated circuit 70 shown in FIG. 1. While the discussion relates to filtering techniques, other types of signal processing events are also applicable. A brief discussion will be provided of filtering techniques followed by a discussion of the applicability of waveform

15   capturing to embodiments/arrangements that include these (and/or other) filtering techniques.

Every transmission line (such as the conductor 70 shown in FIG. 1) has a finite bandwidth, and for signal bandwidths that are comparable to or exceed the transmission line (channel) bandwidth, intersymbol interference (ISI) may present

20   a problem. Furthermore, actual transmission lines may have dispersion, whereby different spectral portions of a signal travel at different speeds. This may result in pulse spreading, again leading to intersymbol interference. As an

example, for high data rates such as 10 Gbs (Giga bits per second), the transmission lines may have intersymbol interference. Channel equalization is a method in which a filter is employed at a receiver so as to equalize the channel.

Additionally, digital signals may have relatively sharp square waveforms

5   representing two or more logic levels. However, line capacitance, noise and the like can cause attenuation of the digital signals and a corresponding "rounding" of the sharp transitions between logic levels. Accordingly, upon receipt of a digital signal, the signals may be restored to their original shape by de-attenuating the signal. Similarly, analog signals are often attenuated during transmission. In a

10   variety of applications, analog signals may be restored to their pre-transmission waveforms prior to further signal processing.

Finite impulse response (FIR) filters may be widely used for various applications. One application is a discrete linear equalizer (DLE), which is used to de-attenuate digital and analog signals in communication systems and

15   integrated circuits. Linear equalizers may be used to restore a signal by taking N samples of the signal over a discrete time window, multiplying each successive input sample X_i by a weighting coefficient A_i, and outputting the sum of the products. The successive data outputs of an FIR filter may be calculated as:

$$Y_1 = \sum_{i-1}^{N} A_i X_i$$

20    $$Y_2 = \sum_{i-1}^{N} A_i X_{i+1}$$

$$Y_3 = \sum_{i-1}^{N} A_i\, X_{i+2}$$

and so on. The variable N accordingly may define the number of "stages" in the FIR filter. When N=3, an FIR filter weighs the current signal against two previously received signals and outputs a weighted average digital signal.

5   Optionally, successive samples can be included in the weighted average.

The analog signal filtering accomplished by such weighted averaging can be readily appreciated by considering a 5V analog source signal that includes data points 0V, 0V, 0V, 5V. During transmission, the analog signal attenuates and becomes, in a simplified example, 0V, 0V, 2.5V, 5V. A three stage FIR filter,

10   upon receiving the 2.5V data point, can combine that data point with the weighted products of the two previously received data points. The FIR output may be less than 2.5V by a factor dictated by the weighting constants, and the attenuation of the signal will be thereby counteracted. By appropriate selection of the weighting constants A_i and appropriate post-filtration amplification, the

15   attenuated signal can be restored to its original waveform, or 0V, 0V, 0V, 5V.

Embodiments of the present invention will now be described with respect to waveform capturing when a channel response is modified such as by filtering as discussed above.

FIG. 4 shows an I/O receiver having a filtering and waveform capturing

20   methodology for one channel according to an example embodiment of the present invention. Other embodiments and configurations are also within the

scope of the present invention. This I/O receiver may be an integrated circuit such as described above as well as including additional circuitry to be described below. More specifically, FIG. 4 shows that input ports 404 and 406 may receive an input differential voltage from a transmission line, such as the conductor 70

5 shown in FIG. 1. Features of the filtering and waveform capturing (such as sample-and-hold circuits 406a-406d, voltage-to-current (V-I) converters 408a-408d, current multipliers (I-DAC) 410a-410d, a comparator/latch device 420 and waveform capture logic (430) may all be provided on-die, such as on the integrated circuit 70 shown in FIG. 1. While FIG. 4 only shows one transmission

10 line (or channel) input to the I/O receiver, a system having more than one channel would have numerous I/O receivers capable of performing the operations to be described with respect to FIG. 4. That is, each channel of a system may include similar corresponding filtering components. Each of these separate channels may share a similar comparator/latch device 420 and similar

15 waveform capture logic 430, and/or each channel may include its own comparator/latch device and waveform capture logic.

The sample-and-hold (S&H) circuits 406a-406d may sample and hold the received differential signal received over the channel. Each of the S&H circuits 406a-406d may generally correspond to the sampler 54 shown in FIG. 1. As an

20 example, each S&H circuit 406a-406d may include two switches (e.g., pass gates), each connected to a capacitor, for example, to store the received differential voltage. Other types of S&H circuits are also within the scope of the

present invention. A clock phase generator 440 may provide clock signals at various phases for each of the S&H circuits 406a-406d. For example, the various clock signals are shown as phase signals Phi1-Phi4 input to the S&H circuits 406a-406d, respectively. Each S&H circuit 406a-406d may be coupled to one of

5   the V-I converters 408a-408d. Each of the V-I converters 408a-408d may be coupled to a respective one of the current multipliers 410a-410d. Each of the current multipliers 410a-410d may be associated with a set of control voltages to perform suitable weighting (i.e., current multiplication). That is, a set of control voltages may be applied to each of the current multipliers 410a-410d.

10   Each of the current multipliers 410a-410d may be coupled to the comparator/latch device 420. The comparator/latch device 420 may sum together the outputs of the current multipliers 410a-410d. The comparator/latch device 420 may include an offset mechanism by which to skew a reference current so as to skew the effective voltage within a time slice. In this example,

15   the current may be offset since multiple samples are provided from the current multipliers 410a-410d.

The waveform output from the comparator/latch device 420 may be input to the waveform capture logic (similar to the storage mechanism 140 shown in FIG. 1). The waveform capture logic 430 may perform waveform capturing in a

20   similar manner as discussed above with respect to FIG. 3.

Embodiments of the present invention are applicable to sampling occurring prior to filtering operations. Embodiments of the present invention are

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also applicable to filtering operations occurring before sampling of the signals. For example, a continuous time filter may be provided before sampling circuits (e.g. sample and hold circuits). A continuous time filter may include an amplifier with feedback to equalize the signals on the channel.

5   FIG. 5 is a circuit diagram of a V-I converter and a current multiplier according to an example arrangement. Other arrangements are also possible. FIG. 6 is a circuit diagram of a V-I converter, a current multiplier and a current latch according to an example embodiment of the present invention. Other embodiments are also within the scope of the present invention. For simplicity,

10   only a 2-bit current multiplier is shown although a current multiplier for a different number of bits may also be implemented.

More specifically, FIG. 5 shows a V-I converter 510 coupled to a current multiplier 550. The current multiplier 550 may be considered as a digital-to-analog converter because the currents I^-_{OUT} and I^+_{OUT} at output nodes 560 and

15   570, respectively, are analog signals modulated by control signals D_1, $\overline{D}_1$, D_2 and $\overline{D}_2$ applied to gates of pMOSFETs 552 and 554 in the current multiplier 550.

In FIG. 5, the current multiplier 550 shunts to ground varying amounts of current depending upon the control signals D_1 and D_2. In the particular example shown in FIG. 5, the pMOSFETs 552 may have a channel width-to-length ratio

20   twice that of the pMOSFETs 554. When D_1 and D_2 are both HIGH, then current from the V-I converter 510 is shunted to ground, and the multiplication value is zero. When D_1 is LOW and D_2 is HIGH, then currents at the nodes 560 and 570

receive 1/3 of the current from the V-I converter 510, and the effective

multiplication value is one. When D_1 is HIGH and D_2 is LOW, then 2/3 of the

currents from the V-I converter 510 is passed through to the nodes 560 and 570,

and the effective multiplication value is two. Finally, when both D_1 and D_2 are

5   LOW, then all of the current from the V-I converter 510 is passed through the

current multiplier 550, and the effective multiplication is three. This may realize 2-

bit multiplication.

The difference in voltages at nodes 560 and 570 represent the

multiplication, where the currents are fed into resistive loads 575. In practice, the

10   loads 575 may be realized by active devices. If the voltage at the node 560

subtracted from the voltage at the node 570 represents a weight, then a weight

having an opposite sign may be realized by subtracting the voltage at the node

570 from the voltage at the node 560. The channel width-to-length ratios for the

pMOSFETs used in the current multiplier 550 need not be powers of two. That is,

15   multiplication may be performed in binary arithmetic. More generally, a mapping

may be provided between control signals and currents passed through the

current multiplier, and it is not necessary that this mapping represent any

particular arithmetic.

The FIG. 5 combination of the V-I converter 50 and current multiplier 550

20   realizes a weighting of the input differential voltage to the V-I converter. This

combination of the V-I converter 510 and the current multiplier 550 along with

loads 575 may be realized as a single stage. Utilizing a single stage may help in

filtering high data rate signals. A plurality of such combinations may be employed to realize a FIR (Finite Impulse Response) filter.

FIG. 6 is a circuit diagram of a V-I converter, an I-DAC and a current latch according to an example embodiment of the present invention. Other

5   embodiments and configurations are also within the scope of the present invention. More specifically, the V-I converter 510 may correspond to one of the V-I converters 408a-408d shown in FIG. 4. The current multiplier 550 may correspond to one of the I-DACs 410a-410d shown in FIG. 4. Additionally, the current latch 580 may correspond to the comparator/latch device 420 shown in

10   FIG. 4. Operations of the V-I converter 510 and the I-DAC 550 may be similar as described above with respect to FIG. 5 and thus a discussion of the elements will not be provided again. The current latch 580 receives the signals from output nodes 560 and 570 of the various I-DACs 550. Each of the other I-DACs may be similarly coupled to a respective current latch circuit.

15   FIGs. 7 and 8 are system level block diagrams according to example embodiments of the present invention. Other embodiments and configurations are also within the scope of the present invention. More specifically, FIG. 7 shows a system 600 including integrated circuits 610 and 620, and a network interface 630. The integrated circuit 610 includes a port circuit 612, and the

20   integrated circuit 620 includes a port circuit 622. Each of the port circuits 612 and 622 may include components to perform filtering and waveform capturing similar as discussed above, such as the components shown and discussed

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above with respect to FIG. 4. As shown in FIG. 7, the port circuits 612 and 622 communicate across a channel 602 (or transmission line). The port circuits 612 and 622 may be simultaneous bidirectional data (SBD) port circuits that drive data onto, and receive data from, the channel 602. The channel 602 may include

5   one or more physical conductors.

The integrated circuits 610 and 620 can be any type of integrated circuit capable of including one or more port circuits as shown. For example, either of the integrated circuits 610 or 620 can be a processor such as a microprocessor, a digital signal processor, a microcontroller, or the like. Either integrated circuit

10   can also be an integrated circuit other than a processor such as an application-specific integrated circuit (ASIC), a communications device, a memory controller, or a memory such as a dynamic random access memory (DRAM). For ease of illustration, portions of the integrated circuits 810 and 820 are not shown. The integrated circuits may include more circuitry than illustrated in FIG. 7 without

15   departing from the scope of the present invention.

The network interface 630 may communicate with the integrated circuit 620 over a bus 632. In some embodiments, the network interface 830 may also communicate with the integrated circuit 610 and other integrated circuits (not shown). For example, in some embodiments, the network interface 630 is a card

20   such as a peripheral component interconnect (PCI) card that communicates with other integrated circuits on a system board. The network interface 630 may be any type of network interface that allows the system 600 to communicate on a

network. For example, network interface 630 may allow connection to a wireless network, a wired network, or the like.

FIG. 8 shows an electronic system 700 including a processor 710, memories 720 and 730, and a network interface 630. The processor 710 may

5   includes port circuits 712 and 714, the memory 720 may include port circuits 722 and 724, and the memory 730 may include port circuits 732 and 734. One or more of the port circuits shown in FIG. 8 may include components to perform filtering and waveform capturing similar as discussed above, such as the components shown and discussed above with respect to FIG. 4.

10 The processor 710, the memory 720, and the memory 730 may be configured in a ring such that each device communicates with two others using at least one port circuit. For example, the processor 710 may communicate with the memory 720 using the port circuit 714 coupled to a signal node 702, and also communicate with the memory 730 using the port circuit 712 coupled to the

15 signal node 706. Also for example, the memory device 720 communicates with the memory device 730 using the port circuit 722 coupled to signal node 704.

In some embodiments, the processor 710 is part of one integrated circuit die, the memory device 720 is part of a second integrated circuit die, and the memory device 730 is part of a third integrated circuit die. In these

20 embodiments, each of the integrated circuit dice may be separately packaged and mounted on a common circuit board. Each of the integrated circuits may also be separately packaged and mounted on separate circuit boards

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interconnected by the signal nodes. In other embodiments, the processor 710 and the memory devices 720 and 730 are separate integrated circuit dice packaged together, such as in a multi-chip module.

Systems represented by the various foregoing figures can be of any type.

5 Examples of represented systems include computers (e.g., desktops, laptops, handhelds, servers, tablets, web appliances, routers, etc.), wireless communications devices (e.g., cellular phones, cordless phones, pagers, personal digital assistants, etc.), computer-related peripherals (e.g., printers, scanners, monitors, etc.), entertainment devices (e.g., televisions, radios,

10 stereos, tape and compact disc players, video cassette recorders, camcorders, digital cameras, MP3 (Motion Picture Experts Group, Audio Layer 3) players, video games, watches, etc.), and the like.

Any reference in this specification to "one embodiment," "an embodiment," "example embodiment," etc., means that a particular feature, structure, or

15 characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of such phrases in various places in the specification are not necessarily all referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with any embodiment, it is submitted that it is within the

20 purview of one skilled in the art to effect such feature, structure, or characteristic in connection with other ones of the embodiments. Furthermore, for ease of understanding, certain method procedures may have been delineated as

separate procedures; however, these separately delineated procedures should not be construed as necessarily order dependent in their performance. That is, some procedures may be able to be performed in an alternative ordering, simultaneously, etc.

5   Although embodiments of the present invention have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this invention. More particularly, reasonable variations and modifications are

10   possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the foregoing disclosure, the drawings and the appended claims without departing from the spirit of the invention. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

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